Attorney Docket No.: 18865-45US
Client Reference No.: 17732-1394

PATENT APPLICATION

FLIP CLIP ATTACH AND COPPER CLIP ATTACH ON MOSFET DEVICE

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BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to a chip device and a method of manufacture thereof and more particularly, to a chip device and a method of manufacture thereof that includes direct attachment of a bumped die to a leadframe and coupling of a set of leads to the bump die with a clip.

2. Description Of The Prior Art

Semiconductor power switching devices, and particularly, power MOSFET devices continue to push the lower limits of on-state resistance. While silicon technology has advanced significantly in the past decade, essentially the same decades old package technology continues as the primary packaging means. The epoxy or soldered die attach along with aluminum or gold wire interconnects is still a preferred power device package methodology.

Recently, chip devices have been manufactured and packaged by connecting the die within the device to the leads directly through a low resistance solder connection. By using a second leadframe element and solder to connect the device conductors and the first leadframe, a direct connection is enabled. Furthermore, the size and shape of the second leadframe may be tailored to fit the chip device and to minimize its electrical and thermal resistance.

When gold wire bonding is done on a gate connection within a chip, the use of adhesives will introduce resin bleeds that are difficult to control and can interfere with the gate bond contact integrity. When silver-filled adhesives are used on the source and drain connections, since adhesives do not flow selectively, the resulting device is

generally more prone to source shorting within the gate or drain. Additionally, adhesives generally have inferior electrical conductivity compared to solders.

Recently, copper straps have been used to couple dies to leads. Generally, with such arrangements, more than 60% of the die area is occupied by the copper strap with adhesives underneath the copper strap. This means less mold plastic is available to securely hold the internal assembly. Since a bigger area is allocated for adhesives, this also means more chances for void formation of the chip device.

Finally, general manufacturing processes for chip devices include attaching the backside of the die with epoxy. Generally, such adhesives have inferior thermal and electrical conductivity in comparison to solders.

SUMMARY OF THE INVENTION

The present invention provides a method of making a chip device wherein a bumped die that includes a plurality of solder bumps thereon is provided and a leadframe including source and gate connections is also provided. The bumped die is placed on the leadframe such that solder bumps contact the source and gate connections. A lead rail with a plurality of leads is provided along with a copper clip. The copper clip is attached to a backside of the bumped die with solder paste such that it contacts the drain regions of the bumped die and a lead rail and is further attached along an edge to the lead rail.

In accordance with one aspect of the present invention, the solder paste is placed on the backside of the bumped die prior to attaching the copper clip.

In accordance with a further aspect of the present invention, the solder paste is placed on the copper clip prior to attaching the copper clip.

In accordance with yet another aspect of the present invention, the solder bumps are reflowed prior to attaching the copper clip.

Thus, the present invention provides an improved chip device and a method of making it. The process does not require any wire bonding because the drain connections are directly soldered on the copper clip during solder reflow while the source and gate bumps are directly coupled to the leadframe. The resulting gate connections are more reliable compared to those produced by the gate wire bonding process. Additionally, solder is used for both the source and drain connections, and thus wetting can only happen on the solderable metals making it less probable for gate shorting as both

connections are isolated with non-wettable areas. Additionally, solder alloys have better conductivity compared to adhesives, which leads to lower RDSon performance of the chip device.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred exemplary embodiments, found hereinbelow, in conjunction with reference to the drawings, in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective view of a chip device in accordance with the present invention;

Figure 2 is a schematic side sectional view of a bumped die;

Figure 3 is a perspective view of a leadframe with flux dispensed thereon for manufacturing a chip device in accordance with the present invention;

Figure 4 is an exploded view of the bumped die and the leadframe for manufacturing a chip device in accordance with the present invention; and

Figure 5 is a perspective view of the bumped die and the leadframe coupled to one another.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1 illustrates a chip device 10 in accordance with the present invention. The chip device includes a leadframe 11 that includes a plurality of leads 12 and a separate lead rail 13 that includes a plurality of leads 14. A bumped die 15 is attached to the leadframe. A clip 16 is placed on the bumped die backside and attached thereto. Additionally, an edge 17 of the clip is placed within a v-groove 18 of the lead rail.

As can be seen in Figure 3, bumped die 15 includes a plurality of solder bumps 20, preferably arranged in rows over a source area 21 of the die on a top surface of the die. A solder bump 22 is also placed on a gate area 23 of the die, which is also on the top surface of the die.

Preferably, the bumped die is provided as a single unit.

Die 12 is preferably a one-piece item that is often referred to in the art as a "bumped die." As can be seen in Figure 2, a bumped die includes die 12, "under bump

material" that serves as an intermediate layer 26 between the top surface of the die and solder bump 22, and the solder bumps themselves. Preferably, the under bump material is one of TiW, Cu, Au or an equivalent. In the example illustrated in Figure 2, the under bump material is broken into three layers – Cu plating 26a, sputtered Cu 26b and sputtered Ti 26d.

Figure 3 illustrates leadframe 11 with flux 27 dispensed thereon. The flux may be dispensed, for example, by stamping, with a multi-needle dispense nozzle or any other suitable method known in the art.

The bumped die is preferably flip chip attached on to leadframe 11, i.e, it is "flipped" from a sawn tape onto the leadframe. The bumped die is placed on the leadframe such that gate solder bump 22 contacts the gate connection region 23 on the leadframe while the source solder bumps 20 contact the source connections 21 on the leadframe.

Solder paste 30 is dispensed on a backside of the bumped die and into elongated v-groove 18 in lead rail 13. Clip 16, preferably consisting of copper, is supplied, (preferably in reel form) and pick-and-placed onto the die backside such that edge 17 of the copper clip is placed within the elongated v-groove. Thus, the clip provides contact with the chip's drain regions (which are located on the chip's backside) and couples these drain regions to leads 14 of the lead rail.

In one embodiment of the present invention, during manufacturing of the chip device, after coupling the clip to the backside of the bumped die and the lead rail, a one time reflow of the solder bumps on the bumped die and the solder paste on the die backside is performed. In an alternative embodiment, the solder bumps may be reflowed after flip chip attaching the bumped die to the leadframe and then a second reflow is performed after placing the copper clip on the die backside.

Accordingly, the present invention provides an improved chip device and simple methods for manufacturing it. The manufacturing process does not require any wire bonding because the drain connections are directly soldered on the copper clip during solder reflow while the source and gate bumps are directly coupled to the leadframe. The resulting gate connections are more reliable compared to those produced by the gate wire bonding process. Additionally, solder is used for both the source and drain connections, and thus wetting can only happen on the solderable metals making it less probable for gate shorting as both connections are isolated with non-wettable areas.

Additionally, solder alloys have better conductivity compared to adhesives, which leads to lower RDSon performance of the chip device.

Although the invention has been described with reference to specific exemplary embodiments, it will appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.